



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,354	01/04/2002	Peter Schalter	112153.125	7032

7590 03/25/2005
Peter M. Diciara
Hale and Dorr LLP
60 State Street
Boston, MA 02109

EXAMINER

FLYNN, KIMBERLY D

ART UNIT	PAPER NUMBER
----------	--------------

2153

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/038,354

Applicant(s)

SCHULTER ET AL.

Examiner

Kimberly D Flynn

Art Unit

2153

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Widget et al (U.S. Patent No. 6,640,251 hereinafter Widget) in view of Aditya (U.S. Patent No. 5,918,021).

In considering claims 1 and 5, Widget discloses the system and method of implementing the address resolution protocol (ARP) in a computing platform having a plurality of processors (see Abstract), comprising:

While Widget discloses the building of an independent based Virtual Private LAN over a multicast enabled IP backbone using stateless tunnels and optional VPLS traffic forwarding (see col. 1, lines 46-49), Widget does not disclose the particular steps of defining the topology of the Ethernet network to be emulated (virtual) on the computing platform. Nonetheless, defining the topology of a Switched Ethernet Network is well known as evidenced by Aditya. In similar art Aditya discloses a system and method for dynamic distribution of data packets through multiple channels that includes a Switch Ethernet Network comprising the following:

the topology including processor nodes and a switch node (see Aditya, col. 1, lines 24-27); assigning a set of processors from the plurality to be processors to act as the processor

Art Unit: 2153

nodes; assigning a processor to act as the switch node (See Aditya fig. 1, (150) (col. 1, lines 28-36); assigning virtual MAC addresses to each processor node of the emulated Ethernet network (see Aditya, col. 1, lines 56-62); allocating virtual interfaces over an underlying physical network to provide direct software communication from each processor node to each other processor node, wherein each virtual interface has a corresponding identification (see Aditya, col. 1, lines 62-67 through col. 2, lines 1-6);

Given the teachings of Aditya, it would have been obvious to a person having ordinary skill in the art to modify the system disclosed by Widget to include the Switched Ethernet Network taught by Aditya in order to provide a network that provides a load balancing scheme operable to distribute the data traffic (i.e. ARP request packets and responses) load equally among the communication channels. Therefore the claimed limitation would have been an obvious modification.

Widget further discloses:

a processor node communicating an ARP request to the switch node, wherein the ARP request includes an IP address (col. 5, lines 43-47);

the switch node communicating the ARP request to all other processor nodes in the emulated Ethernet network (col. 5, lines 47-52 and lines 57-58);

a processor node that is associated with the IP address issuing to the switch node an ARP reply that contains the virtual MAC address of the processor node associated with the IP address (col. 6, lines 1-5);

the switch node receiving the ARP reply and modifying the ARP reply to include a virtual interface identification (VPN Id) for a virtual interface that the processor node issuing the

Art Unit: 2153

ARP request should use for subsequent communication with the processor node associated with the IP address (col. 6, lines 17-26).

In considering claims 2 and 6, the combined system of Widget and Aditya discloses that the underlying physical network is a point-to-point mesh connecting the plurality of processors (see Aditya col. 4, lines 13-21).

In considering claims 3 and 7, the combined system of Widget and Aditya discloses that a subset of the processors are organized as a cluster and that one of the processors in the cluster is a load balancing processor node (see Aditya Abstract and col. 5, lines 61-67 through col. 5, lines 1-5), and that when any processor in the cluster issues the ARP request, the switch node modifies the reply to include the virtual interface identification for the load balancing processor node (see Widget col. 6, lines 17-26).

In considering claims 4 and 8, the combined system of Widget and Aditya discloses that the switch node is in communication with an external IP network, and that the act of communicating an ARP reply includes identifying that the ARP reply is from a processor node in the platform (see Widget col. 6, lines 2-21).

Conclusion

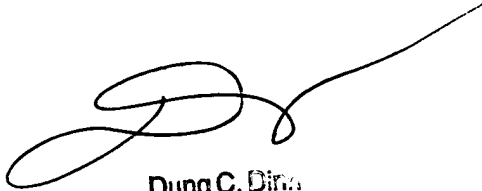
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly D Flynn whose telephone number is 571-272-3954. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glen Burgess can be reached on 703-305-4792. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kimberly D Flynn
Examiner
Art Unit 2153

KDF



Dung C. Dinh
Primary Examiner